REMARKS

The Applicants thank the Examiner for his thorough review of the application, the allowance of claims 1, 13 and 31, and indication of allowability of claims 3-4, 8-10 and 14.

In section 20 of the Office Action, the Examiner indicates that claims 3-4, 8-10 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. This is not understood. Claims 3, 8 and 14 are dependent from claim 1. Claim 4 is dependent from claim 3 (and also from claim 1). Claims 9-10 are dependent from claim 8 (and also from claim 1). Since claim 1 has been allowed (see section 19), there is no need to rewrite these claims into independent form.

What the Examiner really means might be that claims 3-4, 8-10 and 14 would be allowable if the informalities described in sections 8-12 of the Office Action are corrected. These informalities have been corrected (details see below) and the Applicants believe that claims 3-4, 8-10 and 14 are now in condition for allowance.

In section 4 of the Office Action, the Examiner objects to the drawings, suggesting that a legend "Prior Art" should be added to Figures 1A and 1B. Figures 1A and 1B have been amended accordingly. The Applicants believe that this objection has been overcome.

In section 7, the Examiner objects to the abstract, suggesting that it should not be longer than 150 words. The abstract has been amended

accordingly and is now less than 150 words.

In sections 9-12, the Examiner objects to claims 3, 8, 14 and 34 due to a few informalities. These claims have been corrected. In particular, the term "0" at claim 3, line 4 has been deleted. At claim 8, lines 1-2, the phrase "the first and the second ends" has been amended to "the first end and the second end." At claim 14, lines 2-3, the phrase "the sixth doped region" has been amended to "a sixth doped region". At claim 34, line 5, the phrase "the first and second doped regions" has been amended to "the first doped region and the second doped region." The Applicants believe that objections to these claims have been overcome.

35 USC 112 Rejections

In sections 14-15, the Examiner rejects claims 2 and 38 under 35 USC 112, second paragraph, asserting that the feature that a capacitor is coupled between a pad and the first doped region (as recited by claims 2 and 38) is in conflict with the feature that the first doped region is electrically floated in the well region (as recited by claim 1). The Applicants respectfully disagree.

The phrase "electrically floated" means that there is no DC power coupled to the P-type doped region when power is applied to an IC chip. This definition of "electrically floated" is well known in the prior art. For example, please refer to the definition of "floating well" in US Patent No. 6,154,059, No. 5,907,249, No. 5,844,425, No. 6,147,511, No. 6,414,518, No. 5,969,541, No. 5,151,619, No. 5,576,635, No. 6,333,643, No. 5,543,733,

No. 6,344,758, No. 6,407,790 and No. 5,635,861. Generally, an element can be coupled to the electrically floated p-type doped region and does not destroy its electrically floated region if no DC coupling between the p-type doped region and any power supply is introduced. Consequently, the p-type doped region is still in the electrically floated state even if a capacitor is coupled to the p-type doped region because no DC coupling would occur between the p-type doped region and the power supply.

In sections 14 and 16, the Examiner rejects claim 36 under 35 USC 112, second paragraph. Since the features recited in claim 36 is not shown in the elected figures, claim 36 needs not to be examined at this time.

35 USC 102(b) Rejections

In sections 17-18, the Examiner rejects claims 34-35 and 37 under 35 USC 102(b) as being anticipated by Ham (US Patent No. 5,903,420). The grounds for this rejection are respectfully traversed.

Ham does not disclose, suggest, or teach, *inter alia*, the following features recited by claim 34 of the present application:

"a third doped region of the first conductive type, **electrically floated** in the well region, wherein the first node is electrically coupled to the first doped region and the second node is electrically coupled to the second doped region."

In section 18 of the Office Action, the Examiner asserts that the doped region 46 of Ham is electrically floated. The Applicants respectfully

disagree. The doped region 46 in Ham is coupled to V_{SS} through the P-well 22 or coupled to the V_{DD} through the N-well 24 (see e.g. Figs. 6-7 and col. 4, lines 17-20). Thus, the doped region 46 has DC paths coupled to V_{SS} or V_{DD} and is, by definition (see the definition of "electrically floated" above), not "electrically floated".

MPEP 2131 states that a "claim is anticipated only if **each and every element** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," quoting *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). Since Ham does not disclose the elements stated above, the Applicant believes that claim 34 of the present application is patentable over Ham. Claims 35 and 37 are also patentable over Ham, at least by virtue of their dependency from claim 34. Moreover, these dependent claims are patentable by virtue of the additional features cited therein.

The Applicant believes that all pending claims are in condition for allowance and respectfully requests so.

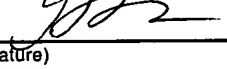
The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account

no. 12-0415.

Enclosed please find a copy of Troy Guangyu Cai's Notice of Limited Recognition under 35 CFR 10.9(b) to prepare and prosecute patent applications wherein the patent applicant is a client of Ladas & Parry, and the attorney of record in the applications is a registered practitioner who is a member of Ladas & Parry.

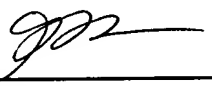
I hereby certify that this correspondence is being deposited with the United States Post Office with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231 on August 29, 2002
(Date of Deposit)

Troy Guangyu Cai
(Name of Person Signing)


(Signature)

8/29/02
(Date)

Respectfully submitted,



Troy Guangyu Cai
Attorney for Applicant
LADAS & PARRY
5670 Wilshire Boulevard, Suite 2100
Los Angeles, California 90036
(323) 934-2300

Appendix A

Marked-up Copy of the Amended Claims

3. (Amended) The output buffer of claim 1, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the second end of the resistor [0] and the source being coupled to the second power line.

8. (Amended) The output buffer of claim 1, wherein the first [and the second ends] <u>end and the second end</u> are respectively comprised of a fourth doped region of the second conductivity type and a fifth doped region of the second conductivity type.

14. (Amended) The output buffer of claim 1, wherein the substrate is coupled to the second power line through [the] <u>a</u> sixth doped region.

34. (Amended) An electrostatic discharge protection circuit coupled between a first node and a second node, comprising:

a substrate of a first conductive type;

a first doped region and a second doped region of a second conductive type formed in the substrate, the first [and second doped regions] <u>doped region and the second doped region</u> being spaced apart enabling a channel region formed in between;

a well region of the second conductive type, formed in the substrate; and

a third doped region of the first conductive type, electrically floated in

the well region, wherein the first node is electrically coupled to the first doped region and the second node is electrically coupled to the second doped region.

Appendix B

Marked-up Copy of the Amended Abstract

[The] An output buffer [of the present invention comprises a pull up circuit and] with a pull down circuit. [The pull up circuit is coupled between a first power line and a pad.] The pull down circuit is coupled between a second power line and [the pad is comprised of] a pad, and has a resistor, a diode and an electrostatic discharge protection component. The resistor deposited on the substrate of a first conductivity type [is comprised of] includes a well region of a second conductivity type [and has a first end and a second end]. [The first end is a forth doped region of the second conductivity type and coupled to the pad.] The resistor and the electrostatic discharge protection component are connected in series between the pad and the second power line. The diode is formed in the well region, construct by the PN junction formed between a first doped region of the first conductivity type and the well region. [The electrostatic discharge component is coupled between the second end and the second power line.] The first doped region is electrically floated in the well regions. [Because the first doped region and the first end are not connected directly, there is no latch-up issue occurring in normal circuit operations.] During an electrostatic discharge event, the [first end] pad is instantaneously connected to the first doped region which will help to boost the turn-on of the electrostatic discharge circuit, and further enhance the electrostatic protection effect.